DAZZLER

SCHEMATIC & FOIL DIAGRAMS

MAINTENANCE MANUAL

Cromemco Dazzler™ BOARD No. 1

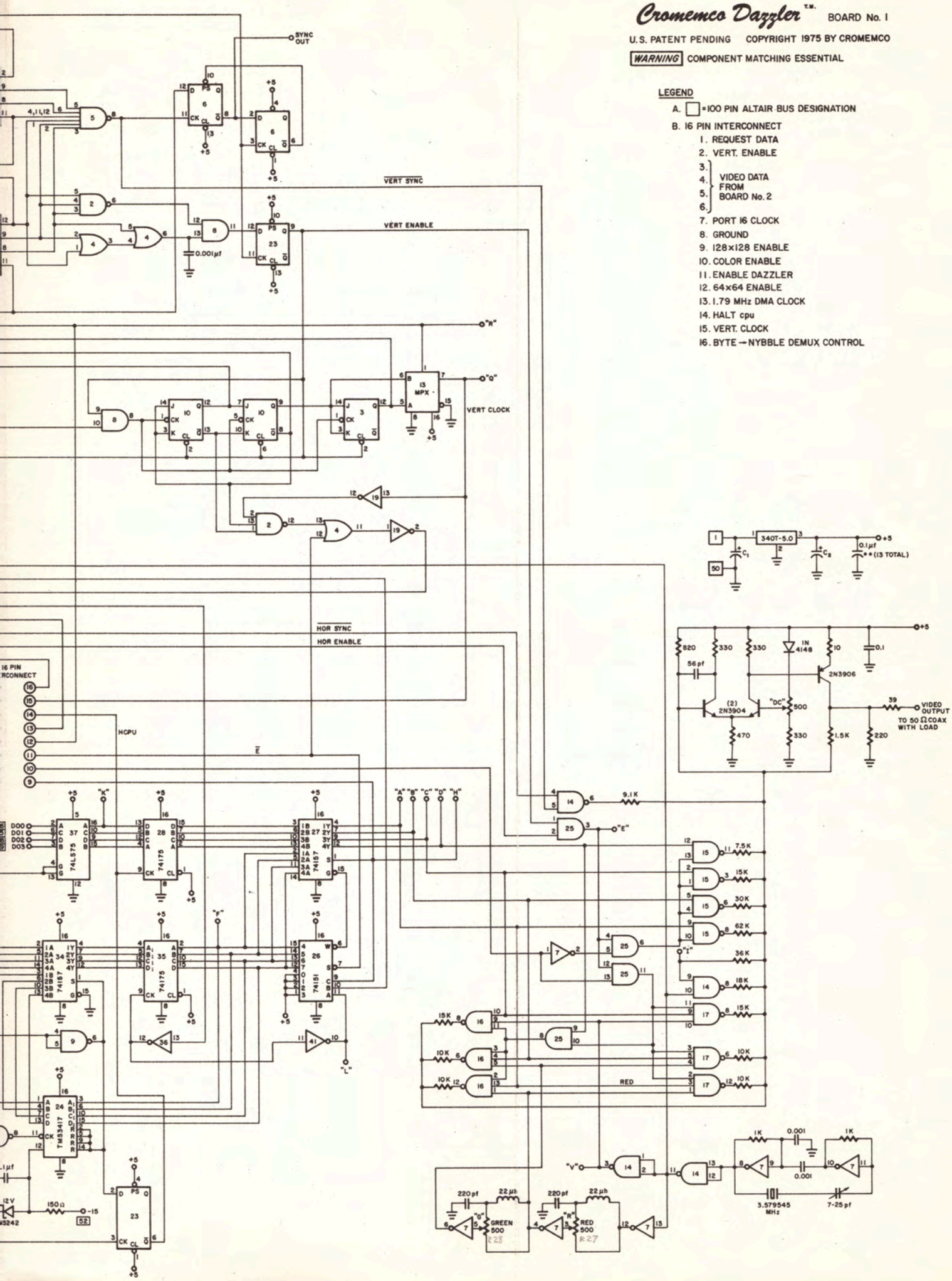
WARNING COMPONENT MATCHING ESSENTIAL

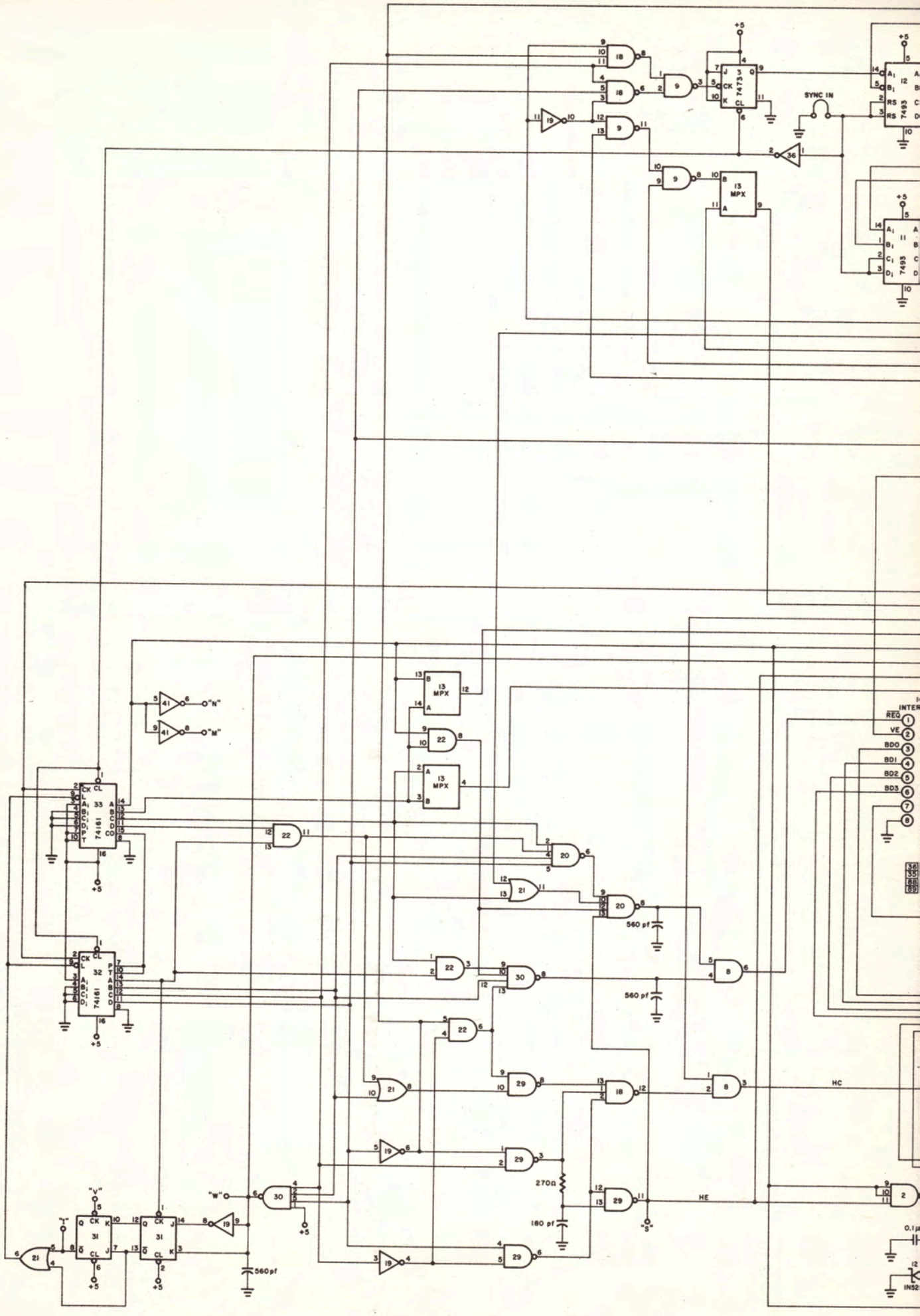
LEGEND

A. □ = 100 PIN ALTAIR BUS DESIGNATION

B. 16 PIN INTERCONNECT

1. REQUEST DATA
2. VERT. ENABLE
3. } VIDEO DATA FROM BOARD No. 2
4. }
5. }
6. }
7. PORT 16 CLOCK
8. GROUND
9. 128×128 ENABLE
10. COLOR ENABLE
11. ENABLE DAZZLER
12. 64×64 ENABLE
13. 1.79 MHz DMA CLOCK
14. HALT cpu
15. VERT. CLOCK
16. BYTE → NYBBLE DEMUX CONTROL

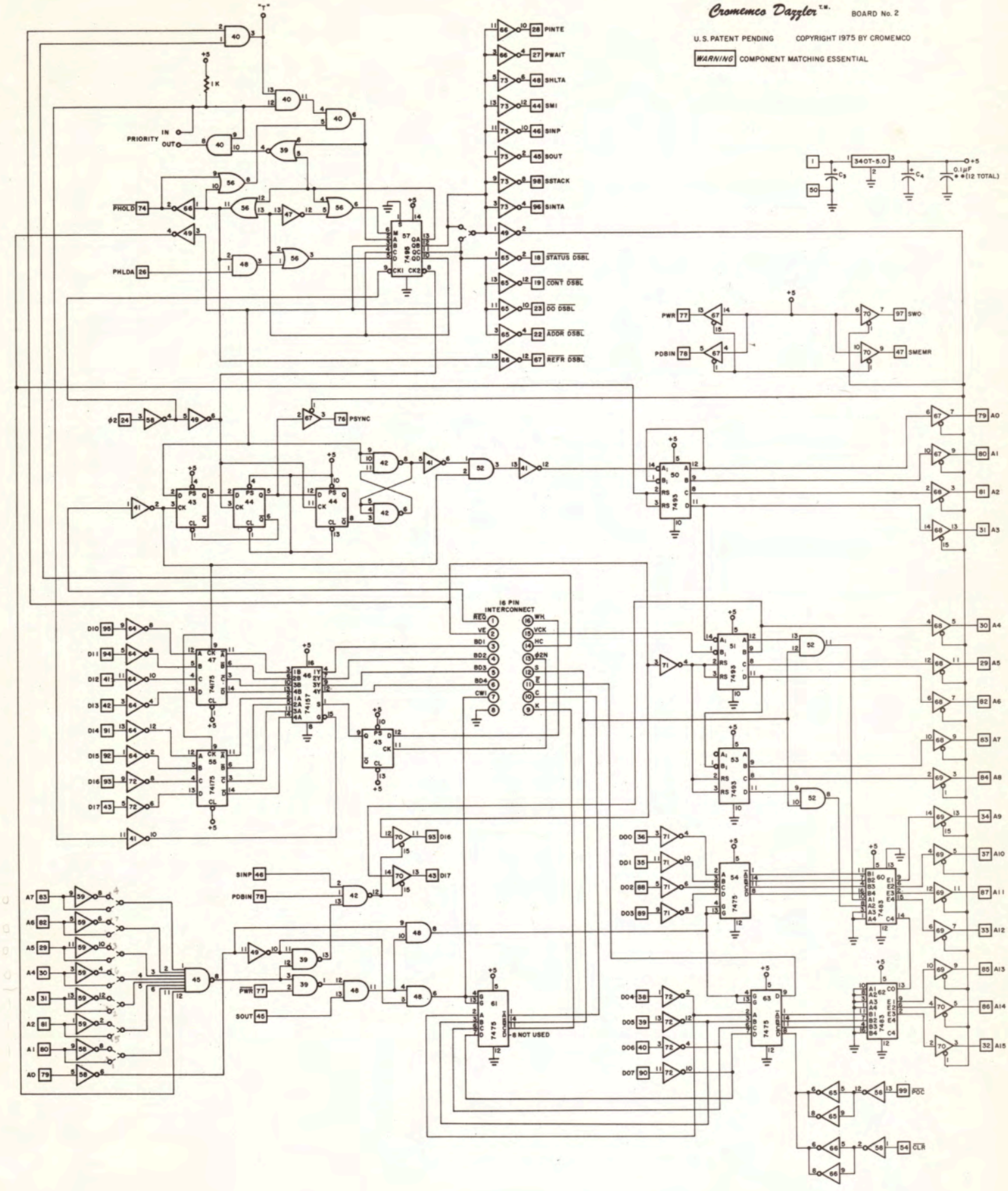


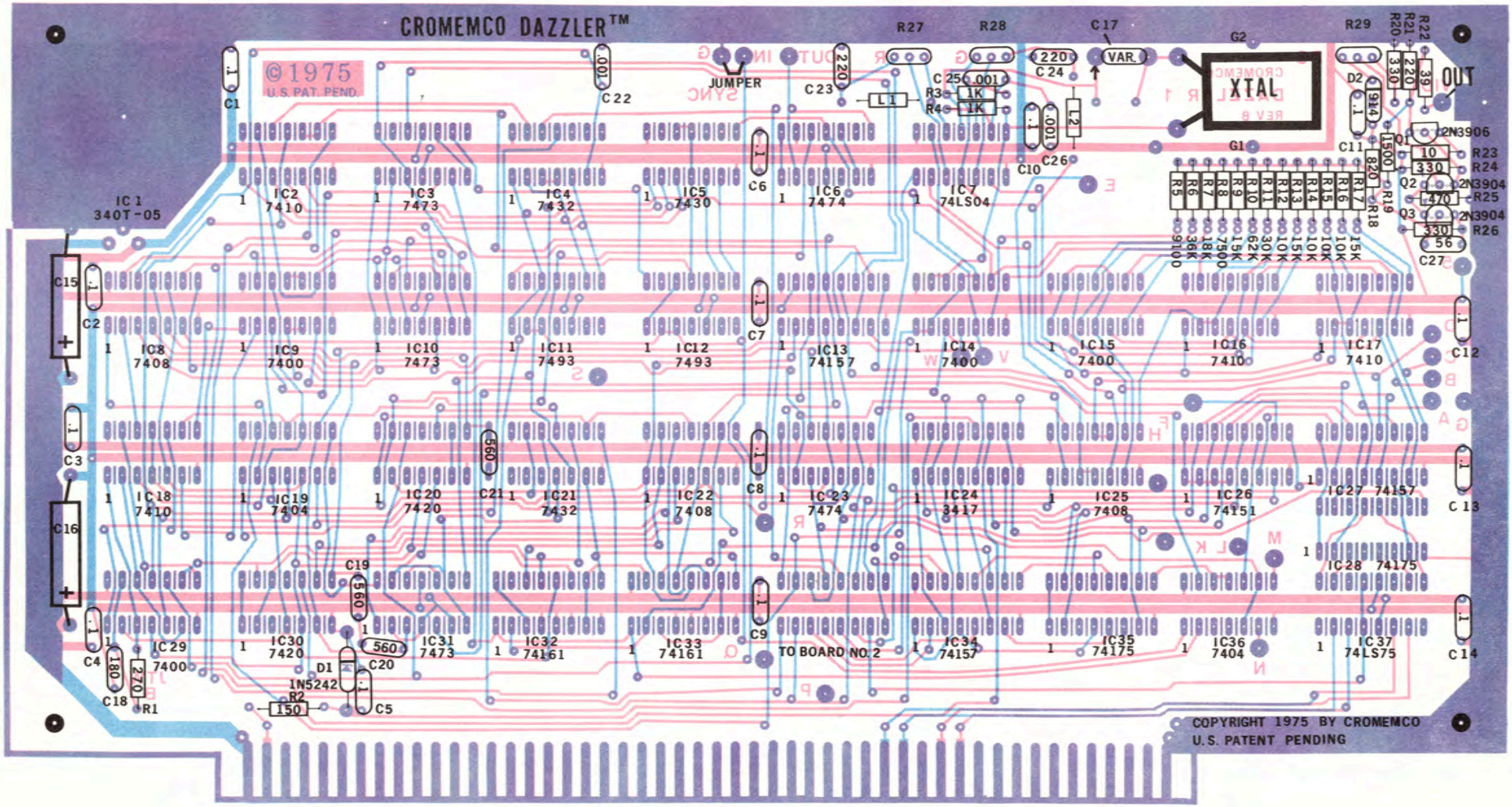

SYNC IN
"N"
"M"
"V"
"W"
"S"
"I"
560 pf
270Ω
180 pf
0.1 μ
HC
HE
INTER
REQ
VE
BD0
BD1
BD2
BD3
IN52
+5
7473
7493
74161
13 MPX

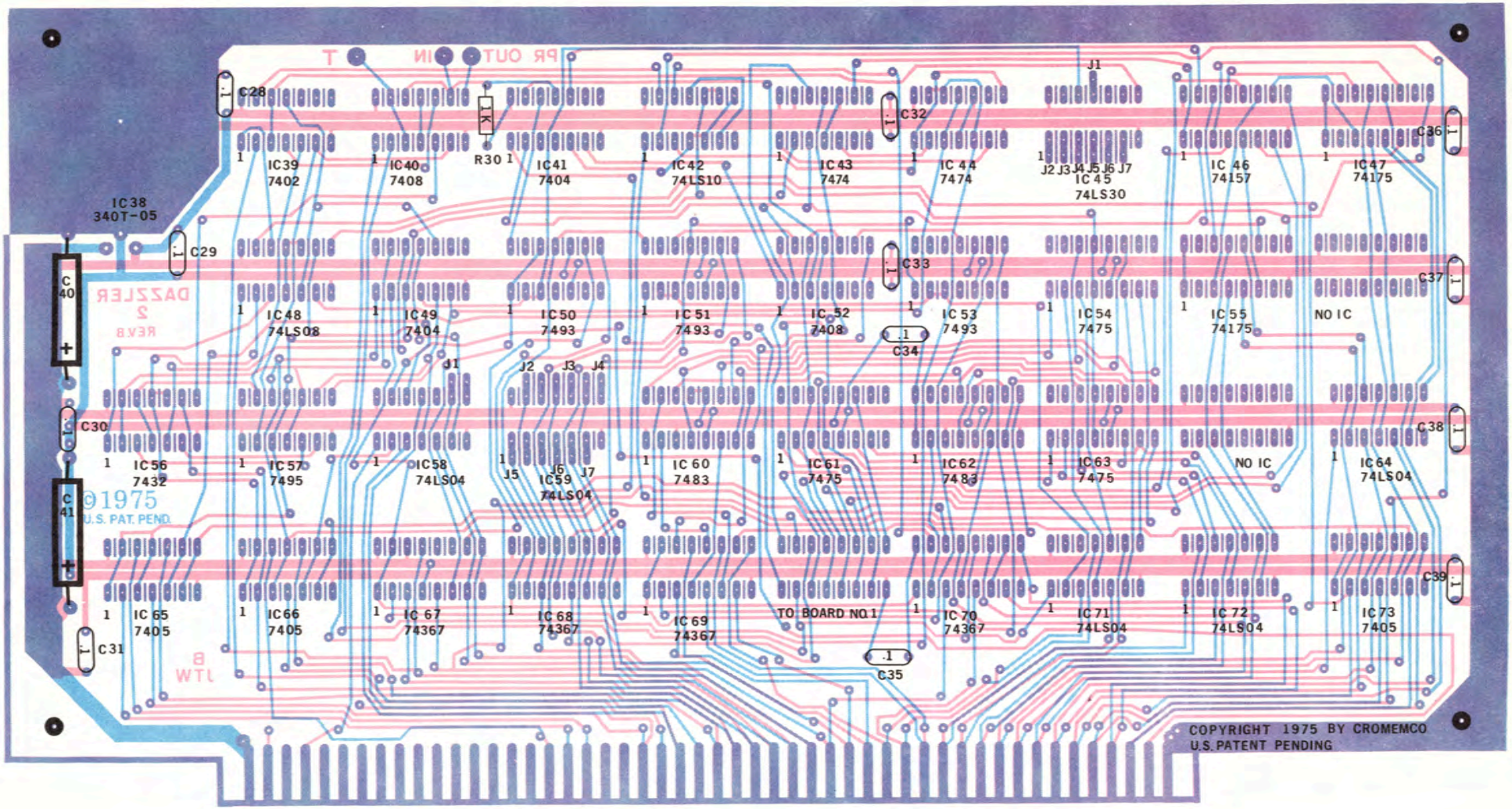
Cromemco Dazzler™ BOARD No. 2

U.S. PATENT PENDING COPYRIGHT 1975 BY CROMEMCO

WARNING COMPONENT MATCHING ESSENTIAL




CROMEMCO DAZZLER™
©1975
U.S. PAT. PEND.
JUMPER
XTAL
OUT
IC 1
340T-05
IC2 7410
IC3 7473
IC4 7432
IC5 7430
IC6 7474
IC7 74LS04
IC8 7408
IC9 7400
IC10 7473
IC11 7493
IC12 7493
IC13 74157
IC14 7400
IC15 7400
IC16 7410
IC17 7410
IC18 7410
IC19 7404
IC20 7420
IC21 7432
IC22 7408
IC23 7474
IC24 3417
IC25 7408
IC26 74151
IC27 74157
IC28 74175
IC29 7400
IC30 7420
IC31 7473
IC32 74161
IC33 74161
IC34 74157
IC35 74175
IC36 7404
IC37 74LS75
2N3906
2N3904
2N3904
D1 1N5242
TO BOARD NO. 2
COPYRIGHT 1975 BY CROMEMCO
U.S. PATENT PENDING


C28
R30 1K
IC38 340T-05
C29
C40
C41
C30
C31
IC39 7402
IC40 7408
IC41 7404
IC42 74LS10
IC43 7474
C32
IC44 7474
J1
J2 J3 J4 J5 J6 J7
IC45 74LS30
IC46 74157
IC47 74175
C36
C33
C37
IC48 74LS08
IC49 7404
IC50 7493
IC51 7493
IC52 7408
C34
IC53 7493
IC54 7475
IC55 74175
NO IC
C38
IC56 7432
IC57 7495
IC58 74LS04
IC59 74LS04
IC60 7483
IC61 7475
IC62 7483
IC63 7475
NO IC
IC64 74LS04
C39
IC65 7405
IC66 7405
IC67 74367
IC68 74367
IC69 74367
TO BOARD NO 1
IC70 74367
IC71 74LS04
IC72 74LS04
IC73 7405
C35
©1975
U.S. PAT. PEND.
COPYRIGHT 1975 BY CROMEMCO
U.S. PATENT PENDING

1/13/76

CROMEMCO DAZZLER Debugging Hints

Equipment Required

1) VTVM or VOM
2) Triggered sweep oscilloscope, preferably DC-5MHz or more, with an external sync input.
3) Frequency counter (optional)
4) Altair 8800 and color TV set with direct video adapter

Procedure

1) Measure the output of each regulator (IC1 & IC38) to be between +4.75 and +5.25 VDC, with less than .1VPP of 60 or 120Hz ripple. If low voltage or excessive ripple exists, check that primary power at regulator input is always >7V, and check IC1 & 38.
2) Measure point "V" with oscilloscope and verify a ~3VPP square wave at 3.579545MHz. The counter can be used to set the frequency with the 7-25pf trimmer to an accuracy of ±500Hz or better.
3) Measure IC7P4&6 to also see ~3VPP square wave at 3.579MHz.
4) Measure point "W" to verify a 4.5 us wide pulse going from +3 to 0 at a 15.98 KHz rate. If not present, check IC's 32, 33, 21, 19, 31, 30, 36, and sync jumper.
5) Measure IC5P8 to verify a .25ms wide pulse going from +3 to 0 at a 62Hz rate. If not present, check IC's 3, 9, 18, 19, 11, 12, 5, 36, and sync jumper.
6) Measure "Sync Out" to verify a 62us wide pulse from 0 to +3 at 62Hz rate. If not present, check IC6.
7) Measure IC23P9 to verify a 12ms wide + pulse at a 62Hz rate. If not present, check IC 2, 4, 8, 23.
8) Measure point "S" to verify a 35.8us wide + pulse at a 15.98KHz rate. If not present, check IC 19, 29.
9) Depress the Altair "CLR" switch & verify IC63P8 is at 0 (or IC4P12 at +3). If does not clear, check IC 58, 63, 66.
10) Load the following Basic Test program into static RAM, starting at address 0 in the Altair and start execution at 0 with the RAM protected. If it won't reset or load, go to A.

loc 0:	076	333	303
	200	377	000
	323	323	000
	016	017	

11) Stop and run the program several times to verify that it stays in the address range 0 to 12_8. If not, or if it won't execute, go to A.

12) With the program in (10) executing, the DAZZLER is enables to display the first portion of memory, with the sense switches controlling output port 017. Verify the following switch control responses:

DØ to IC37P16	D4 to IC61P1
D1 to IC37P10	D5 to IC61P14
D2 to IC37P9	D6 to IC61P11
D3 to IC37P15	D7 to IC61P8

If not present, check IC 37, 61, 72, 39, 48, 49, 45, 58, 59.

13) Verify that IC54P1, 14, 11, 8 and IC63P1, 14, 11 are at 0V and IC63P8 is +3V.
If not present, check IC 71, 72, 54, 63, 65, 66, 58, 48.

14) Temporarily change the instruction at loc 1 to 377 and execute. Verify that IC54P1, 14, 11, 8 and IC63P1, 14, 11, 8 are at +3. If not, check same IC's as in (13). Restore loc 1 to 200 & Run.

15) Stop execution. Verify IC63P8 is +3. Depress CLR switch and verify IC63P8 is now 0V. Put back in RUN. If does not clear, check IC 58, 66.

16) Set sense SW D5=0. Verify IC60P9, 6, 2, 15 and IC62P9, 6, 2 are 0. Temporarily change instruction at loc 1 to 377 and execute. Verify IC60P9, 6, 2, 15 and IC62P9, 6, 2 are at +3. If incorrect action, check IC 52, 60, 62. Restore loc 1 to 200 & Run.

17) Measure IC18P12 and verify a 47us wide + pulse with 62.5us period (15.98KHz). If not present, check IC 18, 21, 22, 29.

18) Connect the scope for external + sync and obtain sync from IC23P9. Measure IC2P12 and verify a burst train of 313us wide pulses from +3 to 0 at a 62.5Hz burst rate, for a total of 32 pulses/burst. Pulse leading edges are spaced 375us. If not present, check IC 2, 3, 8, 10, 13, 19.

19) Observe that setting sense SW D5=1 doubles the number of pulses. Leave D5=0. If not, check IC 3, 13.

20) Measure IC23P6 and verify a burst train of 47us wide + pulses with a 62Hz burst rate. The pulse leading edges should be spaced 250us for a total of 32 pulses/burst, with pulses spaced 62.5us between the bursts. If not present, check IC 9, 23.

21) Observe that setting sense SW D5=1 doubles the number of pulses in the slower portion. Leave D5=0.

22) Measure point "T" to verify a + pulse train burst at a 62Hz rate consisting the slower portion of the waveform in (20). If not, check IC 40.

23) Connect the scope external + sync to point "T" and set the time base to 5us/div so "T" is + during most of visible trace. Measure IC8P6 to verify a burst of pulses from +3 to 0 occurring while"T" is positive.

For D5=0, there should be 33 pulses of width 280ns with 2.23us between leading edges. For D5=1, there should be 65 pulses 280ns wide, spaced 1.11us except for the first pair spaced 2.23us. Leave scope sync on "T". If not correct, check IC 8, 20, 21, 22, 30, 32, 33.

24) Measure IC57P12 to verify a + pulse each time pulse at "T" occurs, with a leading edge delay of 1-5us and a trailing edge delay of .5-1us. If not present, check IC 39, 40, 47, 48, 49, 56, 58, 66, 57. Also check for signals on PHOLD and PHLA, and priority input greater than +3.

25) Measure IC41P12 to verify a pulse train similar to IC41P1, except with the first pulse deleted for either position of D5. If not present, check IC 41, 42, 43, 44, 49, 52, 58. CAUTION: Note IC 44 is specially selected. Use of a non-selected part may require adding 560pf from IC44P5 to ground to allow proper circuit operation.

26) Measure IC50P12, 9, 8, 11 to verify that the horizontal address counter operates in a binary fashion while "T" is high. IC51P12 operates only if D5=1. If not operating, check IC 50, 51, 49.

27) Measure IC 51P9, 8, 11 and IC53P9, 8, 11 to verify Binary operation of the vertical address counter. IC53P11 operates only if D5=1. Use "T" for scope sync. If not correct, check IC 51, 52, 53, 71, 13.

23) If the static RAM at 0 being read out by the DAZZLER was not cleared to 0 prior to loading and execution of the test program, it should contain a random pattern of 1's and 0's. Measure IC47P11, 6, 3, 14 and IC 55 P11, 6, 3, 14 to verify random data reception while "T" is high. If not present, check IC 47, 55, 64, 72.

29) Measure IC43P9 to verify presence of a square wave with period .5us for D5=1 and 1.11us for D5=0. If not present, check IC 13, 43.

30) Measure IC46P4, 7, 9, 12 to verify the presence of random data when "T" is high. If not present, check IC 41, 46.

31) Measure IC24P11 to verify bursts of 64 pulses from +3 to 0, pulses are a square wave of .56us period, with bursts beginning every 62.5us. If not present, check IC2.

32) Set D6=0. Verify point "H" is at 0. If not, check IC 61.

33) Measure points A, B, C, and D to verify presence of random data while "T" is high. If not present, check IC 13, 34, 35, 36, 26, 27, 49, 67, 70, 68, 69.

34) Measure points A,B,C,D to verify similar random data occur in the intervals when T is low. If not present, check for -12V at IC24P12, and check IC 24, 34.

35) Set D4, D5, and D6=0 on sense switches. Measure IC25P6 to verify +3V. If not present, check IC7, 25, 61.

36) Set D4=1 and verify +3 at IC25P11 and 0 at IC25P6. If not, check IC 7, 25.

37) With D4=0, measure IC15P3, 6, 8, 11 to verify presence of the random memory data. Set D4=1 and verify all IC 15 outputs are approximately +3.

38) With D4=1, measure IC16P6, 8, 12 and IC17P6, 8, 12 to verify presence of the random memory data modulated by the 3.58 mHz color subcarrier. If not present, check IC 16, 17, 25.

39) Measure IC14P6 to verify presence of a composite + sync pulse train containing 15.98KHz and 62Hz pulses. If not present, check IC 14.

40) Using point "W" for scope sync, verify presence of a 3.58MHz burst at IC14P8 occurring just after the horizontal sync pulses on IC14P6. If not present, check IC 14.

41) Connect a 50 ohm load to the video output. Set D4=D5=D6=0. Adjust the 500 ohm "DC" pot in the video amplifiers so the most negative portion of the waveform (sync tips) is at +0.5VDC across the 50 ohm load. The more positive portions of the waveform may reach to +1.5VDC. If not possible, check the resistor values, transistors, and diode.

42) Connect the video output to a color TV direct video input through 50 ohm coax with a termination. An illuminated square consisting of a patchwork of many colors should fill the center of the screen if D4=1, with D4=0 producing a picture in shades of grey. D5 should control whether 32 or 64 squares are in each direction. Setting D6=1 will blank out the screen unless at least one of DØ, D1, or D2 are ON.

43) If only the first line of each square appears correct, check IC 24, 34.

44) If all or part of the squares in a line are duplicated from left to right, or lateral jitter appears in the image, check IC44. Try adding 560pf from IC44P5 to gnd.

45) If some type of symmetry or duplication occurs in the display of a static RAM whose contents should be random, check IC 49,67, 68, 69, 70.

46) If the memory doesn't read out, check IC 67, 70.

47) When measuring any particular signal, keep in mind the fact that a PCB short can cause extraneous added pulses.

A) Measure IC57P12 and verify it stays 0V. If not, check IC 40, 47, 48, 56, & 57. If point "T" is staying at +3V, remove IC 40 and connect IC40P6 to ground. If IC57P12 is still not 0V, check for a 2MHz square wave at IC57P8, 9.

B) With IC57P12 at 0V, attempt steps 9, 10, & 11 again. If unsuccessful, check IC 49, 65, 66, 67, 68, 69, 70, 73. Continue at (9). If IC 40 was

left out, replace it between steps 21 & 22, and add a shorting jumper from IC57P12 to ground. Remove the shorting jumper before step 24.

48) If two IC outputs are accidentally shorted together by the PCB, two important effects occur:
   a) Since most gates have greater pull down capability than pull-up, the result is the logical OR of the two separate, desired signals.
   b) At the times when one gate is pulling up and the other is pulling down, the logic signal will be in the range of 0.4 to 1.0V instead of the usual logic 0 range of 0 to 0.4V.

49) Gate outputs are never exactly 0V or +5V unless there is a direct short.